



**BDS Deliverable 3:**

**Prototype Intra-Train Feedback Stabilisation and Scanning System**

R. Apsimon, P.N. Burrows, C. Clarke, B. Constance, H. Dabiri Khah, T. Hartin, C. Perry,  
J. Resta Lopez, C. Swinson, John Adams Institute, Oxford University, UK;

G.B. Christian, ATOMKI, Debrecen, Hungary;

A. Kalinin, STFC Daresbury Laboratory, UK

December 18 2008

Abstract: We present deliverable 3 in the BDS work package.

A number of fast beam-based feedback systems are required at the International electron-positron Linear Collider (ILC). At the interaction point (IP) a very fast system, operating on nanosecond timescales within each bunchtrain, is required to compensate for residual vibration-induced jitter on the final-focus magnets by steering the electron and positron beams into collision. A pulse-to-pulse feedback system is envisaged for optimising the luminosity on timescales corresponding to 5 Hz. Slower feedbacks, operating in the 0.1 – 1 Hz range, will control the beam orbit through the Linacs and Beam Delivery System. Here we present the prototype intra-train feedback stabilisation and scanning system.

The key components of the system are beam position monitors (BPMs) for registering the beam orbit; fast signal processors to translate the raw BPM pickoff signals into a position output; feedback circuits, including delay loops, for applying gain and taking account of system latency; amplifiers to provide the required output drive signals; and kickers for applying the position (or angle) correction to the beam. A schematic of the IP intra-train feedback is shown in Figure 1, for the case in which the beams cross with a small angle; the current ILC design incorporates a crossing angle of 14 mrad.

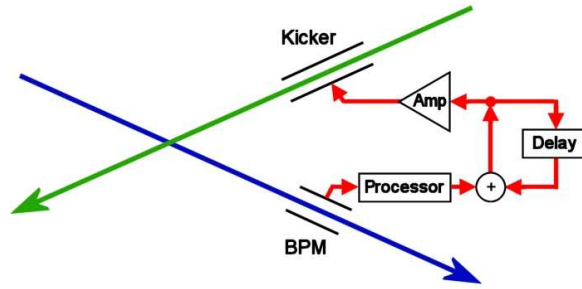


Figure 1: schematic of intra-train feedback stabilisation and scanning system.

Critical issues for the intra-train feedback performance include the latency of the system, as this affects the number of corrections that can be made within the duration of the bunchtrain, and the feedback algorithm. We have designed all-analogue feedback system prototypes in which our aim was to reduce the latency to a few tens of nanoseconds, thereby demonstrating applicability for ‘room temperature’ Linear Collider designs with very short bunchtrains of order 100ns in length, such as CLIC [1]. We achieved total latencies (signal propagation delay + electronics latency) of 67ns (FONT1) [2], 54ns (FONT2) [3] and 23ns (FONT3) [4].

For the ILC prototype we have built a digital system that incorporates a digital feedback processor based on a state-of-the-art Field Programmable Gate Array (FPGA). The use of a digital processor will allow for the implementation of more sophisticated algorithms which can be optimised for possible beam jitter scenarios at ILC. However, a penalty is paid in terms of a longer signal processing latency due to the time taken for digitisation and digital logic operations. This approach is feasible for ILC given the long, multi-bunch train, which includes parameter sets with c. 3000/6000 bunches separated by c. 300/150ns respectively.

A schematic of the FONT4 ILC feedback system prototype [5] and the experimental configuration in the ATF extraction beamline is shown in Figure 2. The layout is functionally equivalent to the ILC intra-train feedback system. An upstream dipole corrector magnet can be used to steer the beam so as to introduce a controllable vertical position offset in stripline BPM ML11X. The BPM signal is initially processed in a front-end analogue signal processor. The analogue output is then sampled, digitised and processed in the digital feedback board to provide an analogue output correction signal. This signal is input to a fast amplifier that drives an adjustable-gap stripline kicker [6], which is used to steer the beam back into nominal vertical position. BPMs ML12X and ML13X can serve as independent witnesses of the beam position.

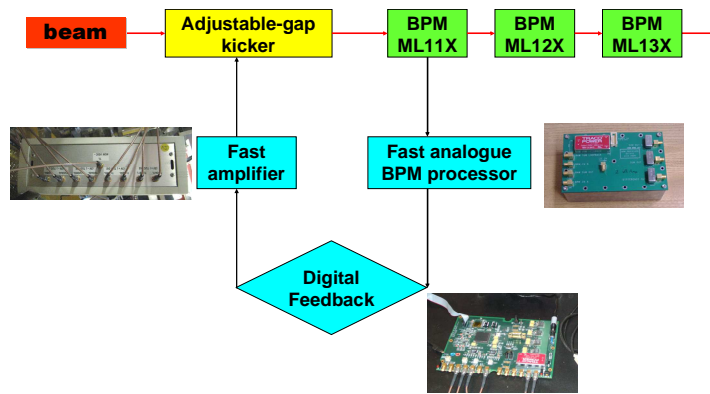


Figure 2: Layout of FONT4 at the ATF extraction beamline showing the relative locations of the kicker, BPMs and the elements of the feedback system.

FONT4 has been designed as a bunch-by-bunch feedback with a latency goal of less than 140ns. This meets the minimum ILC specification of c. 150ns bunch spacing, as well as the smallest spacing allowed at ATF. This will allow measurement of the first bunch position and correction of both the second and third ATF bunches. The correction to the third bunch is important as it allows test of the ‘delay loop’ component of the feedback, which is critical for maintaining the appropriate correction over a long ILC bunchtrain.

The design of the front-end BPM signal processor is based on that for FONT3. The top and bottom (y) stripline BPM signals were added and subtracted using a hybrid, to form a sum and difference signal respectively. The resulting signals were band-pass filtered and down-mixed with a 714 MHz local oscillator signal which was phase-locked to the beam. The resulting baseband signals are low-pass filtered. The hybrid, filters and mixer were selected to have latencies of the order of a few nanoseconds, in an attempt to yield a total processor latency in the range 5-10ns. The measured latency is around 10ns [5].

The custom digital feedback processor board is shown in Figure 3. There are two analogue signal input (output) channels in which digitisation is performed using Analog Devices ADCs (DACs) which can be clocked at up to 105 (210) Ms/s. The digital signal processing is based on a Xilinx Virtex4 FPGA which can be clocked at up to 500MHz. The FPGA is clocked with a 357 MHz source, derived from the ATF master oscillator and hence locked to the beam. Logic operations are triggered with a pre-beam signal. The ADC/DAC are clocked at 357/4 Ms/s. The analogue BPM processor output signal is sampled at the peak to provide the input signal to the feedback.

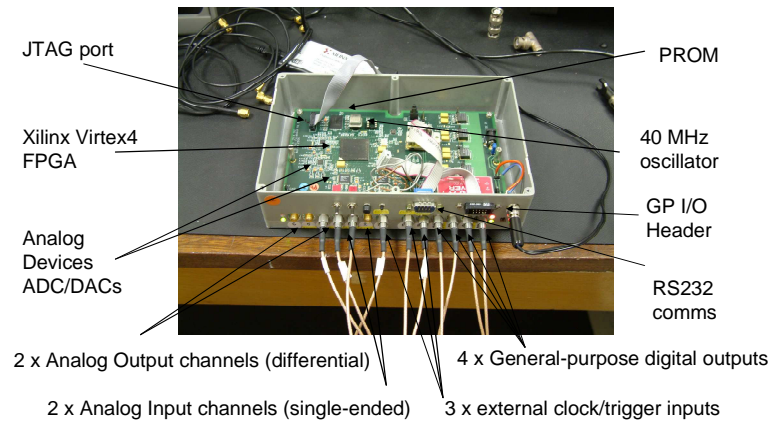


Figure 3: FONT4 digital feedback board.

The gain stage is implemented via a lookup table stored in FPGA RAM, alongside the reciprocal of the sum signal for charge normalisation. The delay loop is implemented as an accumulator on the FPGA. The output is converted back to analogue and used as input to the driver amplifier.

The driver amplifier was manufactured by TMD Technologies [7], a UK-based RF company. The amplifier was specified to provide  $\pm 30\text{A}$  of drive current into the kicker, whose striplines were shorted at the upstream end (nearer the incoming beam). The risetime, starting at the time of the input signal, was specified as  $35\text{ns}$  to reach 90% of peak output. The output pulse length was specified to be up to 10 microseconds. Although current operation is with only 3 bunches in a train of length  $c. 300\text{ns}$ , it is planned in future to operate ATF with extracted trains of 20 or 60 bunches with similar bunch spacing; the design allows for this upgrade.

We report results of the most recent beam tests, performed in May 2008. The beam was steered successively into different vertical positions spanning a range of about  $\pm 200$  microns centred around nominal zero. An example is shown in Figure 4. The data shown are the averages over 11 pulses. The feedback is seen to make a ‘perfect’ correction of bunch 3 by an appropriate gain choice. It should be noted, however, that the bunchtrain is not straight, there being a sagitta of order 100 microns between the incoming bunches, and this complicates the operation of the feedback system. Nevertheless the system works as expected. The latency was measured to be  $c. 140\text{ns}$  [5].

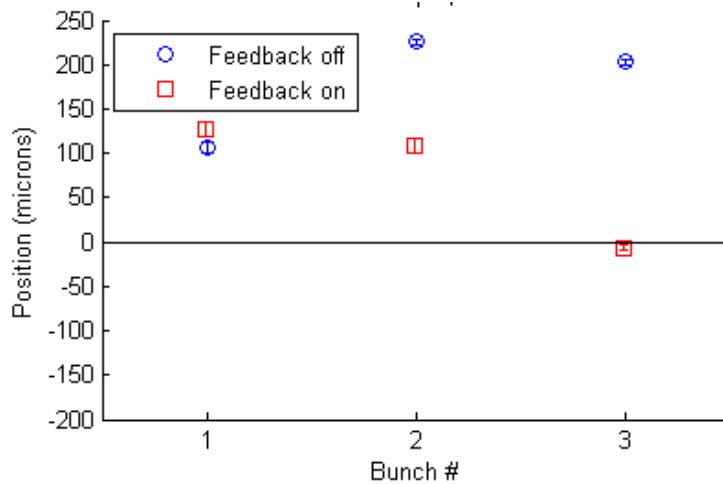


Figure 4: Beam position vs. bunch number:

## Acknowledgement

This work is supported by the Commission of the European Communities under the 6th Framework Programme "Structuring the European Research Area", contract number RIDS-011899, and by the UK Science and Technology Facilities Council (STFC).

## References:

- [1] CLIC: <http://clic-study.web.cern.ch/CLIC-Study/>
- [2] P.N. Burrows et al, Proceedings PAC03, Portland, Oregon, May 2003, p. 687.
- [3] P.N. Burrows et al, Proceedings EPAC04, Lucerne, July 2004, p. 785.
- [4] P.N. Burrows et al, Proceedings PAC05, Knoxville, TN, May 2005, p. 1359.
- [5] P.N. Burrows et al, Proceedings EPAC06, Edinburgh, UK, June 2006, p. 849.  
P.N. Burrows et al, Proceedings PAC07, Albuquerque, NM, June 2007, p. 416.  
R. Apsimon et al, Proceedings EPAC08, Genoa, June 2008, p. XXX.
- [6] <http://acfahep.kek.jp/subg/ir/feather/index.html>
- [7] [www.tmdtechnologies.co.uk](http://www.tmdtechnologies.co.uk)